A PARTIAL INTER-LOCKING METAL CONTACT STRUCTURE FOR SEMICONDUCTOR DEVICES AND METHOD OF MANUFACTURE

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to semiconductor and integrated circuit structures generally and, particularly to a novel metal contact structure and method that exhibits enhanced mechanical integrity and electromigration resistance in BEOL interconnects comprising the structures.

Description of the Prior Art

[0002] As millions and millions of devices and circuits are squeezed on a semiconductor chip, the wiring density and the number of metal levels are both increased generation after generation. In order to provide low RC for high signal speed, low-k dielectric and copper lines become necessary. The quality of thin metal wirings and studs formed by a Damascene process is extremely important to ensure yield and reliability. Two major problems encountered in this area today are poor mechanical integrity of deep submicron metal studs, and unsatisfied electro-migration resistance in BEOL interconnects. The problem becomes more severe when porous low-k material is used.

[0003] A metal line and via formation according to the prior art is described in U.S. Patent No. 5,098,860 issued to Chakravorty, et al., March 24, 1992 entitled "Method of fabricating high-density interconnect structures having tantalum/tantalum oxide layers". This reference describes a interconnect structure 10 as illustrated in Figure 1 including a top metal line, 16, connected to a bottom metal line, 11, through a metal via, 18, and these metallic interconnects are embedded in a low-k dialectic material, 12. Additionally, these metal interconnects are enclosed with diffusion barriers, including

liners 14 and 15 in order to prevent out-diffusion of the metallic atoms into the dielectric material, 12, and include a cap insulator layers 13 and 17.

[0004] In another prior art teaching, described in U.S. Patent No. 6,383,920 by Wang, et al. entitled "Process for Enclosing Via for Improved Reliability in Dual Damascene Interconnects", a via contact comprising a crown-shaped liner is described. In this reference, which is directed to a dual damascene process, a resulting interconnect structure 20 shown in Figure 2 includes a crown-shaped liner material 25 including liner portions 25a, 25b that extend up to the surface 26 of the upper metal wire level 16. In this structure, current that flows along the interlevel wire 16 and into the stud must pass through higher resistive liner 25 and suffers a crowding effect. This not only creates reliability concerns, but also slows down the signal propagation speed of the structure.

[0005] Moreover, each of the metal and stud formations taught in the prior art as shown in Figure 1 and Figure 2 fail to improve stud mechanical strength, nor to enhance electromigration effect. For example, as depicted in the perspective view of a portion of a conventional multi-layer conducting interconnect structure 400 shown in Figure 4(B), there is provided four metal lines, 41, 43, 45 and 47, and their corresponding contact vias 42, 44 and 46. Metal line 41 and 45 are parallel to each other, but perpendicular to both metal lines 43 and 47. In this layout, contact vias all are aligned perfectly to the underlying metal wires. As shown in Figure 4(B), the locations in the structure depicted by dotted lines represent that either the contact via metal connects directly with the adjoining metal underlayer, or alternately, the diffusion barrier layer forms the interface between the via and the adjoining metal layer. In this conventional structure 40 shown in Figure 4(B), locations 48 where the formed liner contacts the metal layer always have weak mechanical strength due to the essential thermal mismatch between metal and dielectrics. This failure may be revealed as broken barrier materials, which will eventually degrade the reliability of the circuits.

[0006] As a further example, a Figure 5(B) depicts a portion of a conventional multi-layer conducting interconnect structure 50, however, in this conventional embodiment, the vias are misaligned to the underneath metal lines. Thus, as shown in Figure 5(B), vias 52 and 56 are misaligned to the underneath metal lines 51 and 55 respectively as shown in the Figure 5(B). Like the case in Figure 4(B), in Figure 5(B), the locations in the structure depicted by dotted lines represent that either the contact via metal connects directly with the adjoining metal underlayer, or alternately, the diffusion barrier layer forms the interface between the via and the adjoining metal layer. In this conventional structure 50 shown in Figure 5(B), locations 58 where the formed liner contacts the metal layer always have weakened mechanical strength.

[0007] Moreover, as depicted in the cross-sectional view of a conventional conducting interconnect structure 90 in Figure 9(A), there exists essentially two possible paths of electron migration from a contact via 98 into an adjoining upper level metal line 96: a first path 92 representing the one along the metal and the diffusion barrier interface; and, a second path 91 representing the one inside the bulk metal line 96. Since the electromigration resistance is always higher in path 91 than in path, 92, the resulting electromigration issue is much more considerable in path 92 than in path 91. By forcing electrons flow from the contact 98 to the upper metal line 96 through path 91 and avoiding path 92 the circuit reliability is enhanced significantly.

[0008] It would thus be highly desirable to provide a method and structure for improving the mechanical strength of submicron metal studs and enhancing electromigration resistance in high wiring density semiconductor chips.

SUMMARY OF THE INVENTION

[0009] It is an object of the present invention to provide a method and structure for improving the mechanical strength of submicron metal studs in multi-level interconnect high wiring density semiconductor structures.

[0010] It is an object of the present invention to provide a method and structure for enhancing electromigration in multi-level interconnect high wiring density semiconductor structures.

[0011] In the satisfaction of the above objects, a "Lego"- like inter-locking contact structure and method for fabricating the same is provided for high wiring density semiconductors characterized in that the contact liner formed in the via extends only partially into the adjacent wire level. As a consequence, current crowding and related reliability problems associated with conventional prior art interconnect structures is avoided and structural integrity of the stud structure is enhanced.

[0012] A "Lego"- like stud structure with a "crown" of liner extending partially into a next wire level significantly enhances the mechanical strength of metal interconnect. Besides, it also improves the electro-migration resistance of BEOL due to a relatively high liner resistance which forces electrons to go around the fence and then flow down through the stud. In this case, current crowding effect is prevented resulting in less electromigration.

[0013] According to an aspect of the invention, there is provided a semiconductor interconnect structure and method of manufacture, the structure comprising first level of metal conductor and second level of metal conductor and one level of insulator material formed therebetween, the structure further comprising a dielectric metal contact via formed at the insulator material level for electrically connecting the first metal and second metal conductors, wherein the metal contact via includes metal liner material surrounding the metal contact via, a portion of said metal liner extending partially into an adjacent metal level of the first and second metal levels, in interlocking relation therewith to enhance mechanical strength of the semiconductor interconnect structure and improve electromigration resistance.

[0014] According to another aspect of the invention, there is provided a semiconductor capacitor device and method of manufacture, the device comprising a first layer of conductor material forming a bottom node and a first insulator material layer formed thereon; a plurality of metal contact studs formed on said first layer of conductor material having lined sidewall portions extending upwards above a top surface of said insulator material; a second insulator layer formed on said first insulator material layer and conforming to said upward extending lined sidewall portions and, a second layer of conductor material forming a top node on top said second insulator layer, wherein an area density of said capacitor device is improved.

[0015] According to a further aspect of the invention, there is provided a semiconductor heat sink structure and method of manufacture, the heat sink structure comprising: a first layer of heat sink material; a layer of insulator material formed on the first heat sink material layer; a plurality of contact studs extending upwards from the heat sink material layer through the insulator material layer, the contact studs having sidewall portions and filled with heat sink material to improve area density of the heat sink structure.

[0016] Advantageously, the novel "crown" shape of the Lego-like liner structure that is fabricated to extend in an upward direction may be employed for other integrated circuit applications including forming capacitor (e.g., MIMCAP) and heat sink structures due to its increased surface area.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Further features, aspects and advantages of the structures and methods of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings where:

[0018] Figure 1 depicts a cross-sectional view of a conventional interconnect structure 10 including a top metal line, 16, connected to a bottom metal line, 11, through a metal via 18;

[0019] Figure 2 depicts a cross-sectional view of a interconnect structure 10 according to the prior art wherein a liner extends up to a surface of the adjoined metal layer;

[0020] Figure 3 is a cross-sectional diagram of a first embodiment of the invention showing the formed contact liner in the via extending only partially into the adjacent wire level 16;

[0021] Figures 4(A)- 4(C) depict various top (Figure 4(A)) and cross-sectional views (Figures 4(B)-4(C)) of an interlevel connect structure according to the prior art (Figure 4(B)) and the inventive interlevel connect structure having the Lego-like inter-locking contact via structure according to a first embodiment of the invention as shown in Figure 4(C);

[0022] Figures 5(A)- 5(C) depict various top (Figure 5(A)) and cross-sectional views (Figures 5(B)-5(C)) of an interlevel connect structure according to the prior art (Figure 5(B)) and the inventive interlevel connect structure having the Lego-like inter-locking contact via structure according to a second embodiment of the invention as shown in Figure 5(C);

[0023] Figures 6 to Figure 8 depict variations of Lego-contact structures with Figure 6 depicting a via formation implementing a dual Damascene process with a perfect alignment; Figure 7 depicting a via formation with a slight misalignment; and, Figure 8 depicting a via formation implementing a single Damascene process;

[0024] Figures 9(A) and 9(B) depict two possible paths of electron migration from a contact via into the upper level metal line according to the prior art in (Figure 9(A)) and according to the current invention (Figure 9(B));

[0025] Figures 10(A)-10(H) depict a process sequence for improving the dislocation-related leakage in strained-layer MOSFETs. fabricating a "lego"- like inter-locking contact structure according to the present invention.

[0026] Figures 11(A)- 11(G) depict a step-by-step fabrication process 99 to form an improved MIMCAP device having increased surface area according to the invention; and,

[0027] Figures 12(A)-12(E) depict a method 300 for fabricating an improved heat sink structure for improving the heat dissipation from semiconductor packages/chips according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0028] According to the invention, a method of forming new studs having "Lego"-like inter-locking contact structure is proposed. A schematic representation of a cross-sectional interconnect structure 30 according to the current invention is shown in Figure 3.

[0029] As illustrated in Figure 3, the interconnect structure 30 includes a top metal line, 36 connected to a bottom metal line, 31, through a metal via, 38, and these metallic interconnects are embedded in a low-k dialectic material, 32. Additionally, these metal interconnects are enclosed with diffusion barriers, including a contact liner 34 and 35, and a cap insulator, 37, in order to prevent out-diffusion of the metallic atoms into the dielectric material, 32. However, as shown in Figure 3, the diffusion barrier portions 35a and 35b formed in the via extends only partially into the adjacent wire level 36.

[0030] A comparison of the structure and a conventional one is illustrated in Figures 4(A)- 4(C). In Figure 4(A) a top view is presented of the prior art interlevel connect structure and the inventive interlevel connect structure 40' of the invention having the

Lego-like inter-locking contact via structure according to the invention as shown in Figure 4(C).

[0031] In both cross-sectional perspective views shown in Figures 4(B) and 4(C), there is depicted four metal lines, 41, 43, 45 and 47, and their corresponding contact vias 42, 44 and 46. Metal line 41 and 45 are parallel to each other, but perpendicular to both metal lines 43 and 47. In this layout, contact vias all are aligned perfectly to the underlying metal wires. In the conventional structure 40 shown in Figure 4(B), sites 48 always have weak mechanical strength due to the essential thermal mismatch between metal and dielectrics. This failure may be revealed as broken barrier materials, which will eventually degrade the reliability of the circuits. However, in the structure 40' of Figure 4(C), with a "crown" shape of liner extending only partially upwards into the adjacent conductive layer, the mechanical strength at the locations 49 of Figure 4(C) in structure 40' is significantly enhanced.

[0032] Figures 5(A)-5(C) depict similar views as in Figures 4(A)- 4(C), however, in this case, via 52 and 56 are misaligned to the underneath metal lines, 51 and 55 respectively as shown in the figures. During chip fabrication, this misalignment is observed frequently. Figures 5(B)- 5(C) are the corresponding cross-sectional representations from a conventional structure 50 (Figure 5(B) and the structure 50' Figure 5(C) of the current invention. Because of the existing "crown" shape of liner extending only partially up into the adjacent conductive layer in the structure 50', the locations 59 have better mechanical strength than sites 58 as in Figure 5(A) without the inventive liner shape.

[0033] Figures 6 to Figure 8 depict variations of Lego-contact structures with Figure 6 depicting a via formation 60 implementing a dual Damascene process with a perfect alignment; Figure 7 depicting a via formation 70 with a slight misalignment; and, Figure 8 depicting a via formation 80 implementing a single Damascene process. In the variation of Lego-contact structure 60 shown in Figure 6, a dual Damascene process is implemented to result in perfect alignment of liners 61,62 with liner 62 extending

partially into the upper metal layer 66. However, in Figure 7, with a slight misalignment, the liners 71 and 72 extend to the top surface 77 of the metal wire 76. In Figure 8, the via 84 is formed by using single Damascene process with formed liners 81 and 82 extending partially into the upper metal layer 86 In each structure, the mechanical strength of the interconnects is enhanced. Although, only three structures shown here, it is understood that all other possible combinations of different interconnect structures is contemplated within the scope of the invention.

[0034] With respect to the electron-migration resistance phenomena, unlike the two possible paths of electron migration from a conventional contact via formation shown in Figure 9(**A**), the via formation structure 95 of the invention depicted in Figure 9(**B**) has a feature of preventing or slowing down electromigration by forcing electron flow from path 92 (Figure 9(**A**)) to path 91.

[0035] A step-by-step fabrication process 100 to form the interconnect structure of the invention depicted in Figures 10(A)-10(G) is now described. A post via etch profile in an insulator such as silicon oxide, silicon nitride, TEOS, or other low-k dielectrics, e.g. SiLK, (Coral, Black Diamond, doped-TEOS, and other organic dielectrics and carbon-doped $SiO2$ based dielectrics) etc., 701, is shown in Figure 10(A), wherein the etch opening reaches the underneath metal line702 through the formed cap layer 703. A diffusion barrier material, 711, is then deposited on the patterned wafer as shown in Figure 10(B). Preferred diffusion barrier materials may include, but are not limited to: TiN(Si), TaN, Ti, Ta, W, Ru, WN, TaN/Ta and other like materials including combinations thereof. The liner material may be formed in the opening utilizing conventional deposition processes well known to those skilled in the art, including: CVD, PECVD, ALD, PVD, plating and chemical solution deposition. The thickness of the diffusion barrier liner may vary depending upon the liner material as well as the method used in forming the same. Typically, the liner 711 has a thickness from about 5Å to about 1000 Å and will vary according to the design and process implemented. As shown in Figure 10(C), a spin-on organic material, 721, and a thin oxide liner layer, 722, are used as planerization layers for metal line patterning, and a photoresist mask 723 is

patterned. Figure 10(D) illustrates the resultant profile 730 after patterning to form top metal layer wiring. The structures 60, 80 depicted in of Figures 6 and 8, respectively, will be dependent upon the mask pattern of Figure 10(D) and the resultant etched profile 730 of Figure 10(E). The final etching profile 740 is shown in Figure 10(E) which illustrates the removal of all the resist and filling material 721 utilizing a conventional etch process. A second diffusion barrier, 751, is then deposited as shown in Figure 10(F) to a thickness of 5 Å ~1000 Å. A layer of conductive material 761 is then filled into the patterned features as shown in Figure 10(G). Preferred conductive materials may include, but are not limited to the following metals: Cu, Al, W, Ag and alloys thereof. Finally, Figure 10(G) shows the final profile 776 after removing away extra conductive materials and barrier materials by chemical mechanical polishing (CMP). It is understood that minor variations known to skilled artisans may be implemented to the process such as the employment of further single or dual Damascene processes to result in an interlocking structures as depicted in Figures 8 and 6, respectively.

[0036] As mentioned, the novel "crown" shape of the Lego-like liner structure that is fabricated to extend from the vias in an upward direction partially into an adjacent conductor level may be employed for other integrated circuit applications including improvement in forming a MIMCAP (metal-insulator-metal capacitor) due to increased surface area. A step-by-step fabrication process 99 to form the MIMCAP having increased surface area according to the invention is depicted in Figures 11(A)- 11(G).

[0037] In a first processing step depicted in Figure 11(A), a first insulator layer 110, comprising an oxide, nitride, oxynitride of silicon, or equivalent insulator materials, including high-k or low-k dielectric materials which can be sacrificial, is deposited on top of a first patterned metal 100 serving as a bottom plate of the MIMCAP. Utilizing conventional via patterning, an array of vias 120 is formed as depicted in Figure 11(B). Then, metal liners 130 are formed as depicted in Figure 11(C) using conventional materials and processes as described herein. Next, the metal studs 140 are formed in the formed vias as depicted in Figure 11(D) using conventional materials and processes as described herein. Then, the sacrificial insulator 110 is recessed to a predetermined depth

"d" 150 as shown in Figure 11(E). The depth of recess "d" is variable and depends upon the particular application, materials and processing method but may typically range on the order of several angstroms to thousands of angstroms. It is understood that the deeper the recess, the more surface area, but weaker of the free-standing structure. Then, as depicted in Figure 11(F) using conventional materials and processes, a high-k dielectric material 160 is deposited over the array structure that conforms to extended liners and recesses. Typical high-k dielectric materials that may be used include: TA2O5, (Ba,Sr) TiO3 (BST), SrTiO3 (STO), etc. Finally, a second conductor material, e.g., metal is patterned to form a top plate 170 of the MIMCAP 180 as shown in Figure 11(G).

[0038] For those semiconductor packages/chips including a heat sink structure, the method for fabricating the novel "crown" shape of the Lego-like structure according to the present invention is advantageous for increasing surface area for heat sink application. Thus, a method 300 to improve heat dissipation from semiconductor packages/chips is now described with respect to Figures 12(A)-12(E). With respect to the process for manufacturing an improved heat sink structure, first, as shown in Figure 12(A), an insulating layer 210 is deposited on a heat sink layer 200. Then, as shown in Figure 12(B), the insulating layer 210 is patterned to form one or more trenches 220 which are then filled with a conformal coating of heat sink material 230, as shown in Figure 12(C). Then, in a first embodiment of the heat sink structure, the remaining insulating material of layer 210 is partially removed to a depth, "h", of several angstroms (Å) to thousands of angstroms as shown in Figure 12(D) between the conformal coating of heat sink material 230 to improve heat dissipation and retain mechanical strength. In a second embodiment of the improved heat sink structure as shown in Figure 12(E), the trench openings are filled with a material 240 with desired thermal conductive properties to improve heat removal. It should be understood that the process described with respect to Figures 12(A)-12(E) may be generalized to multilevel build sequences.

[0039] While the invention has been particularly shown and described with respect to illustrative and preferred embodiments thereof, it will be understood by those skilled in

the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention that should be limited only by the scope of the appended claims.